REMARKS

Objections to the specification

The title and the abstract have been objected to due to their inclusion of the term "non-DMA." Applicant has amended the title and the abstract to remove this term, and requests the withdrawal of this objection.

Objections to the drawings

The drawings have been objected to because of the term "non-DMA." Applicant has submitted replacement drawing sheets in which this term has been removed, and requests the withdrawal of this objection.

Claim objections

Claims 1-3, 16-19, and 22 have been objected to because of the term "non-DMA." Applicant has amended these claims to remove this term, and requests the withdrawal of this objection.

Claim rejections

Claims 1-3 and 5-28 have been rejected under 35 USC 102(b) as being anticipated by Yoshiba (4,816,815). Claim 4 has been rejected under 35 USC 103(a) as being unpatentable over Yoshiba in view of Dunn (4,497,036). Claims 1, 16, and 22 are independent claims, from which the remaining pending claims ultimately depend. Applicant submits that at least as amended, claims 1, 16, and 22 are patentable over Yoshiba, such that all the pending claims are patentable at least because they depend from patentable base independent claims.

Claim 1 is discussed as representative of all the independent claims insofar as the present rejection is concerned. Claim 1 has been amended to recite the limitations of claims 10 and 13,

and any claims that depended from claims 10 and 13 have been amended to instead depend from claim 1. Claims 16 and 22 have been amended in a similar manner to claim 1.

Claim 1 is thus now limited to "the display data transfer circuit . . . monitor[ing] changes made to the pixels of the frame buffer memory, and . . . serially transfer[ring] the pixels of the frame buffer memory that have changed to the display." Claim 1 is also now limited to "the frame buffer memory [being] a first frame buffer memory," where the system of claim 1 further comprises "a second frame buffer memory to which the pixels of the first frame buffer memory are copied." As such, claim 1 is limited to "the display data transfer circuit . . . compar[ing] pixels of the second frame buffer memory against the pixels of the first frame buffer memory to determine whether changes have been made to the pixels of the first frame buffer memory."

Therefore, in claim 1 as amended there are two frame buffer memories. The display data transfer circuit monitors changes made to the (first) frame buffer memory, and transfers the pixels that have changed to the display. This is achieved by the display data transfer circuit comparing the pixels of the second frame buffer memory against the pixels of the first frame buffer memory to determine whether any changes have been made to the pixels of the first frame buffer memory.

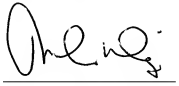
Applicant respectfully submits that these limitations of claim 1 are not disclosed by Yoshiba. In rejecting claim 13, which previously recited the limitation of the display data transfer circuit comparing the pixels of the second frame buffer memory against the pixels of the first frame buffer memory to determine whether changes have been made to the pixels of the first frame buffer memory, prior to the incorporation of claim 13 into claim 1, the Examiner relied upon column 8, line 66 through column 9, line 7 of Yoshiba. However, this part of Yoshiba simply states:

> The signal OBS1 now high level enables the display data buffer 164 and sets the data input/output buffer 122 of the VRAM 24 to a write mode. Then, the data stored in the region 314 of the VRAM 16 are sequentially read out and transferred to the CRT 10 to be displayed thereon, while being transferred to the VRAM 24 to be sequentially written in the region 320. In this manner, the display data from the head address SA to the tail address EA are displayed and, at the same, their copy is developed in the region 320.

Nothing in this portion of Yoshiba states that there is any "comparing" of the pixels of the first frame buffer (i.e., the VRAM 16) to the pixels of the second frame buffer (i.e., the VRAM 24) "to determine whether changes have been made to the pixels of the first frame buffer," in contradistinction to the claimed invention. Applicant has reviewed the rest of Yoshiba as well, and cannot locate any disclosure therein as to the comparing of pixels of one frame buffer memory (i.e., the VRAM 16) to the pixels of another frame buffer memory (i.e., the VRAM 24) to determine whether changes have been made to the pixels of the former frame buffer memory.

Therefore, because Yoshiba does not disclose these limitations, it does not anticipate claim 1 or the other independent claims. The standard for anticipation under 35 USC 102 is that every limitation of a claim must identically appear in a single prior art reference for it to anticipate the claim. (In re Bond, 15 USPQ2d 1566 (Fed. Cir. 1990)) "T]here must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention." (Scripps Clinic & Research Found. v. Genentech, Inc., 18 USPQ2d 1001, 1010 (Fed. Cir. 1991)) In the present situation, not every limitation is found in Yoshiba, and there is a difference between the claimed invention and Yoshiba, such that there is no anticipation.

Respectfully Submitted,



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Michael A. Dryja, Reg. No. 39,662
Attorney/Agent for Applicant(s)

Law Offices of Michael Dryja
1474 N Cooper Rd #105-248
Gilbert, AZ 85233
tel: 425-427-5094

fax: 425-563-2098